Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A CDAC circuit configured for correction of gain errors, said CDAC circuit comprising:

a positive capacitor array comprising N capacitors, said N capacitors having a common side configured for coupling to a pedestal voltage, and another side configured for sampling onto an input signal and a reference signal through control of N switches; and

an additional capacitor having one side configured for coupling to the pedestal voltage, and another side configured to couple to said input signal during sampling to facilitate reduction of a positive full-scale voltage and thus reduce an operating range of said CDAC circuit to control gain.

2. (Original) The CDAC circuit according to claim 1, wherein said additional capacitor can be switched between said input signal and ground to increase an amount of charge sampled to decrease a level of said input signal necessary to achieve full charge levels, and thereby reduce a high-end of said range to less than said reference voltage.

3. (Original) The CDAC circuit according to claim 2, wherein said additional capacitor can be switched between said input signal and said reference signal to provide additional charge back to said CDAC circuit, and thereby adjust a low-end of said range.

4. (Original) The CDAC circuit according to claim 2, wherein said additional capacitor comprises a capacitance value of approximately between 0.5pF and 1.1pF to achieve a range of between approximately 0.3 volts and 2.2 volts.

5. (Original) The CDAC circuit according to claim 2, wherein said positive capacitor array is configured to sample on less than all N capacitors within said positive capacitor array to incrementally increase said range and thereby control gain.

6. (Original) The CDAC circuit according to claim 5, wherein said CDAC circuit samples with said additional capacitor to provide a course adjustment of gain, and said CDAC circuit samples on less than all said N capacitors to provide a fine adjustment of gain.

7. (Original) The CDAC circuit according to claim 1, wherein said CDAC circuit is further configured for offset correction and further comprises:

a negative capacitor array comprising M capacitors, said M capacitors being configured for coupling to an input signal, ground and a reference signal through control of M switches, wherein said negative capacitor array is configured for sampling with at least one of said M capacitors to said reference signal, and a remainder of said M capacitors to ground to facilitate convergence to a desired offset voltage.

8. (Original) The CDAC circuit according to claim 7, wherein said negative capacitor array is configured for incrementally selecting said M capacitors to adjust said offset voltage.

9. (Original) The CDAC circuit according to claim 7, wherein said negative capacitor array can comprise an additional capacitor to facilitate bi-directional adjustment to an offset voltage.

10. (Original) An analog-to-digital converter circuit, said analog-to-digital converter comprising:

a successive approximation register;

a comparator circuit having an output coupled to said successive approximation register;

an output circuit coupled to said successive approximation register; and

a CDAC circuit configured for correction of gain errors, said CDAC circuit coupled to said comparator circuit and comprising:

a positive capacitor array comprising N capacitors, said N capacitors having a common side configured for coupling to a pedestal voltage, and another side configured for sampling onto an input signal and a reference signal through control of N switches; and

an additional capacitor having one side configured for coupling to the pedestal voltage, and another side configured to couple to said input signal during sampling to facilitate reduction of a positive full-scale voltage and thus reduce an operating range of said CDAC circuit to control gain.

11. (Original) The analog-to-digital converter circuit according to claim 10, wherein said additional capacitor can be switched between said input signal and ground to increase an amount

of charge sampled to decrease a level of said input signal necessary to achieve full charge levels, and thereby reduce a high-end of said range to less than said reference voltage.

12. (Original) The CDAC circuit according to claim 11, wherein said additional capacitor can be switched between said input signal and said reference signal to provide additional charge back to said CDAC circuit, and thereby adjust a low-end of said range.

13. (Original) The CDAC circuit according to claim 11, wherein said additional capacitor comprises a capacitance value of approximately between 0.5pF and 1.1pF to achieve a range of between approximately 0.3 volts and 2.2 volts.

14. (Original) The CDAC circuit according to claim 11, wherein said positive capacitor array is configured to sample on less than all N capacitors within said positive capacitor array to incrementally increase said range and thereby control gain.

15. (Original) The CDAC circuit according to claim 14, wherein said CDAC circuit samples with said additional capacitor to provide a course adjustment of gain, and said CDAC circuit samples on less than all said N capacitors to provide a fine adjustment of gain.

16. (Original) The CDAC circuit according to claim 10, wherein said CDAC circuit is further configured for offset correction and further comprises:

a negative capacitor array comprising M capacitors, said M capacitors being configured for coupling to an input signal, ground and a reference signal through control of M switches,

wherein said negative capacitor array is configured for sampling with at least one of said M capacitors to said reference signal, and a remainder of said M capacitors to ground to facilitate convergence to a desired offset voltage.

17. (Original) The CDAC circuit according to claim 16, wherein said negative capacitor array is configured for incrementally selecting said M capacitors to adjust said offset voltage.

18. (Original) The CDAC circuit according to claim 16, wherein said negative capacitor array can comprise an additional capacitor to facilitate bi-directional adjustment to an offset voltage.

19. (Original) A method for correction of gain errors in a CDAC circuit, said method comprising the steps of:

sampling an input signal with at least one capacitor in a capacitor array of a positive side of said CDAC circuit;

sampling said input signal with an additional capacitor to increase an amount of charge sampled, thereby decreasing a level of said input signal necessary to achieve full charge levels and decreasing a range of said CDAC circuit.

20. (Original) The method according to claim 19, wherein said method further comprises the steps of:

sampling said input signal without at least one capacitor of said capacitor array to incrementally increase said range of said CDAC circuit to thereby control gain.

21. (Original) The method according to claim 20, wherein said step of sampling said input signal with said additional capacitor provides a course adjustment, and said step of sampling said input signal without at least one capacitor of said capacitor array comprises a fine adjustment.

22. (Original) The method according to claim 19, wherein said method is configured for correction of offset errors and further comprises the step of:

sampling a reference signal with at least one capacitor in a capacitor array of a negative side of said CDAC circuit;

converging said CDAC circuit to an adjusted offset voltage to correct for offset error.

23. (Original) A CDAC circuit configured for correction of gain errors, said CDAC circuit comprising:

a positive capacitor array comprising N capacitors configured for sampling onto an input signal through control of N switches; and

an additional capacitor configured to facilitate reduction of a positive full-scale voltage and thus reduce an operating range of said CDAC circuit to control gain, said additional capacitor configured for switching between said input signal and ground to increase an amount of charge sampled to decrease a level of said input signal necessary to achieve full charge levels, and thereby reduce a high-end of said range to less than a reference voltage.

24. (Original) The CDAC circuit according to claim 23, wherein said positive capacitor array is configured to sample on less than all N capacitors within said positive capacitor array to incrementally increase said range and thereby control gain.

25. (New) A CDAC circuit configured for correction of gain errors, said CDAC circuit comprising:

a positive capacitor array comprising N capacitors, said N capacitors having a first side configured for coupling to a pedestal voltage, and a second side configured for sampling onto an input signal; and

an additional capacitor having a first side configured for coupling to the pedestal voltage, and a second side configured to couple to said input signal during sampling to facilitate reduction of a positive full-scale voltage.